Most circuit boards have a front or component side, on which all or most of the components are mounted, and a rear or back side, which typically has few, if any, components. The test system 20 shown in Figs. 5-7 includes test terminals formed on the back side of the circuit board and arranged to couple the device to be tested to the circuit board. In the example of Fig. 5, the test terminals are connector pins 25 which are soldered to the back side of the circuit board. The test system 20 includes sockets 23 which are normally arranged to couple memory modules to the front surface of the circuit board 21 (in this example, a mother board). Referring to Fig. 7, however, one of the sockets 23a is removed and the connector pins 25 are formed on the rear surface of the mother board 21 on regions corresponding to the removed socket 23a shown by the dotted line. Alternatively, the connector pins 25 can be formed on the rear surface on regions corresponding to all sockets 23 without removing any of the sockets.

At page 4, line 29 to line 31, Please replace the paragraph with the followings:

The interface board 29 is supported between the interface board 29 and the mother board 21 by supports 33, and fixed to the mother board 21 by fasteners 35, thereby attaching the interface board 29 firmly to the mother board 21.

At page 5, line 13 to line 25, please replace the paragraph with the followings:

As described above, a test system for semiconductor devices according to the present invention tests devices by coupling them to the back side of a circuit board, thereby eliminating interference with CPUs (not shown) or other peripheral components such as the add-in boards 41a, 41b in FIG. 7 or 61a, 61b in FIG. 9. Therefore, the present invention does not require the use of conventional connection boards or extension boards. The present invention also facilitates the use of automatic handling of the semiconductor devices that are to be tested. Accordingly, the present invention reduces the cost of testing semiconductor devices under actual usage conditions. It also eliminates the delay and/or distortion of the electrical signals caused by unnecessary resistance, inductance, and/or parasitical capacitance. Moreover, because the present invention allows the devices to be tested to be coupled to the back side of the circuit board, this provides extra clearance that allows the devices and/or the interface board to be oriented in positions that might otherwise be impossible if they were mounted on the component side.